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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,483	02/10/2004	Sohrab Kianian	2102397-992012	3244

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,483	KIANIAN ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-68 and 75-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-68 and 75-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/12/04 in parent 09/982413* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 66-68 are rejected under 35 U.S.C. 102(b) as being anticipated by Tzeng. As to claim 66, Tzeng, Figure 9, discloses a method of operating a semiconductor memory cell formed in a semiconductor substrate, the memory cell includes a substrate of semiconductor material of a first conductivity type (10), a floating gate (12) disposed over and insulated from a surface of the substrate, and first and second spaced-apart regions (24) and (25) formed in the substrate and having a second conductivity type, with a non-linear channel region therebetween, wherein the channel region defines a path for programming the floating gate with electrons from the second region, the method comprising the steps of: coupling a positive voltage to the floating gate, embodied as raising the control gate typically to 12 volts; and inducing electrons to flow from the second region, through a first portion of the channel region, to inject electrons onto the floating gate (col. 7, line 63 to col. 8, line 4).

As to claim 67, Tzeng, Figure 9, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 68, Tzeng, Figure 9, discloses the channel region first portion extends in a direction substantially perpendicular to the substrate surface.

Claims 66-68 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofmann et al.. As to claim 66, Hofmann et al., Figure 8, discloses a method of operating a semiconductor memory cell formed

in a semiconductor substrate, the memory cell includes a substrate of semiconductor material of a first conductivity type (25), a floating gate (40) disposed over and insulated from a surface of the substrate, and first and second spaced-apart regions (60) and (45) formed in the substrate and having a second conductivity type, with a non-linear channel region therebetween, wherein the channel region defines a path for programming the floating gate with electrons from the second region, the method comprising the steps of: coupling a positive voltage to the floating gate, embodied as applying a positive voltage to the select gate (120)(col. 7, lines 43-45); and inducing electrons to flow from the second region, through a first portion of the channel region, to inject electrons onto the floating gate (col. 7, lines 17-19).

As to claim 67, Hofmann et al., Figure 8, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 68, Hofmann et al., Figure 8, discloses the channel region first portion extends in a direction substantially perpendicular to the substrate surface.

Claims 75-79 are rejected under 35 U.S.C. 102(b) as being anticipated by Tzeng. As to claim 75, Tzeng, Figure 9, discloses a method of operating a semiconductor memory cell formed in a semiconductor substrate, the memory cell including a trench formed into a surface of a substrate of semiconductor material of a first conductivity type (10), first and second spaced-apart regions (24) and (25) formed in the substrate and having a second conductivity type, with the second region formed underneath the trench such that a channel region of the substrate is defined between the first and second regions that extends substantially along a sidewall of the trench and substantially along the substrate surface, a floating gate of electrically conductive material (12) disposed over and insulated from at least a portion of the channel region and a portion of the first region, a control gate of electrically conductive material (31) having a first portion disposed in the trench, and insulation material (30) disposed between the floating gate and the control gate having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col. 8, lines 10-13), the method comprising: coupling a positive voltage to the floating gate; and inducing electrons to flow from the second region, through a first portion of the channel region, to inject electrons onto the floating gate (col. 7, line 63 to col. 8, line 4).

As to claim 76, Tzeng, Figure 9, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 77, Tzeng, Figure 9, discloses the channel region first portion extends in a direction substantially perpendicular to the substrate surface.

As to claim 78, Tzeng, Figure 9, discloses the channel region first portion extends substantially along the sidewall of the trench.

As to claim 79, Tzeng, Figure 9, discloses that the channel region includes a second portion that extends substantially along the substrate surface.

Claims 75-79 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofmann et al.. As to claim 75, Hofmann et al., Figure 8, discloses a method of operating a semiconductor memory cell formed in a semiconductor substrate, the memory cell including a trench (140) formed into a surface of a substrate of semiconductor material of a first conductivity type (25), first and second spaced-apart regions (45) and (60) formed in the substrate and having a second conductivity type, with the second region formed underneath the trench such that a channel region of the substrate is defined between the first and second regions that extends substantially along a sidewall of the trench and substantially along the substrate surface, a floating gate (40) of electrically conductive material disposed over and insulated from at least a portion of the channel region and a portion of the first region, a control gate (120) of electrically conductive material having a first portion disposed in the trench, and insulation material (115) disposed between the floating gate and the control gate having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col. 3, lines 1-2), the method comprising: coupling a positive voltage to the floating gate (col. 7, lines 43-45); and inducing electrons to flow from the second region, through a first portion of the channel region, to inject electrons onto the floating gate (col. 7, lines 17-19).

As to claim 76, Hofmann et al., Figure 8, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 77, Hofmann et al., Figure 8, discloses the channel region first portion extends in a direction substantially perpendicular to the substrate surface.

As to claim 78, Hofmann et al., Figure 8, discloses the channel region first portion extends substantially along the sidewall of the trench.

As to claim 79, Hofmann et al., Figure 8, discloses that the channel region includes a second portion that extends substantially along the substrate surface.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann et al. in view of Wang. Hofmann et al., Figure 8, discloses the invention of claim 75. Hofmann et al., Figure 8, further discloses that the floating gate (40) has a first end disposed over and insulated from the first region, and a second end disposed over and insulated from the channel region. Hofmann et al. does not disclose expressly the floating gate including a sloping upper surface that terminates in a sharp edge that extends toward the control gate. Wang, Figure 2, discloses a floating gate (44) formed in an EPROM with a sloping upper surface that terminates in a sharp edge that extends toward the control gate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the floating gate of Hofmann et al. with the shape of the floating gate of Wang. The motivation for doing so would have been to avoid planarizing the upper surface of the floating gate, thereby preserving the shape of the floating gate as a manufacturing artifact. Therefore, it would have been obvious to combine Wang with Hofmann et al. to obtain the invention as specified in claim 80.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
October 8, 2004